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TECHNIQUES FOR PROGRAMMING AND VERIFYING DATA IN A PROGRAMMABLE CIRCUIT

ABSTRACT OF THE DISCLOSURE

[60] The present invention includes techniques for programming and verifying data in a programmable circuit. Programmable circuits such as PLDs may include a plurality of rows and columns of memory cells. Data is programmed into memory elements associated with the rows and columns. Subsequently, the programmed data may be extracted for verification. A first word line may be selected by first word line address bits in row shift registers. Data programmed into the first word line is loaded into column shift registers for verification during one or more verify steps. During a program step, data is programmed into memory elements in a second word line that is selected by the first word line address bits. The present invention also provides a technique for shifting program data bits into the column shift registers at the same time that verify data bits are shifted out of the column shift registers.